CLAIMS

What is claimed is:

1. A method for testing AC coupled interconnects of a circuit having at least one driving IC and at least one receiving IC that are coupled together by at least one AC interconnection, each IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller, the method comprising the steps of:

shifting an AC test stimulus into the BSCs of the at least one driving IC;

scanning an initiate AC test instruction into the instruction register of both ICs;

performing an execute AC test instruction by moving the TAP controller to the *Run-Test/Idle* state and holding the TAP controller of both ICs in the *Run-Test/Idle* state for the time required to complete execution of the AC test instruction, wherein, during the *Run-Test/Idle* controller state, the at least one driving IC is applying the AC test stimulus to the at least one AC interconnection and the at least one receiving IC is sampling the signal;

transferring the results into the BSCs of the at least one receiving IC; and

scanning out the captured results.

2. The method as defined in claim 1, further comprising the step of evaluating the captured AC test instruction results.

3. The method as defined in claim 1, further comprising the step of generating a second AC test stimulus and repeating the steps of shifting, scanning, performing, transferring and scanning out with the second AC test stimulus.

4. The method as defined in claim 3, further comprising the step of evaluating the captured AC test instruction results for the second AC test stimulus.

5. A system for testing AC coupled interconnects of a circuit having at least one driving IC and at least one receiving IC that are coupled together by at least one AC interconnection, each IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller, the system comprising:

means for shifting an AC test stimulus into the BSCs of the at least one driving IC;

means for scanning an initiate AC test instruction into the instruction register of both ICs;

means for performing an execute AC test instruction by moving the TAP controller to the *Run-Test/Idle* state and holding the TAP controller of both ICs in the *Run-Test/Idle* state for the time required to complete execution of the AC test instruction, wherein, during the *Run-Test/Idle* controller state, the at least one driving IC is applying the AC test stimulus to the at least one AC interconnection and the at least one receiving IC is sampling the signal;

means for transferring the results into the BSCs of the at least one receiving IC; and

means for scanning out the captured results.

6. The system as defined in claim 5, further comprising means for evaluating the captured AC test instruction results.

7. The system as defined in claim 5, further comprising means for generating a second AC test stimulus.

8. The system as defined in claim 7, further comprising means for evaluating the captured AC test instruction results for the second AC test stimulus.

9. A computer-readable medium having stored thereon computer-executable instructions for performing a method for testing AC coupled interconnects of a circuit having at least one driving IC and at least one receiving IC that are coupled together by at least one AC interconnection, each IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller, the method comprising the steps of:

shifting an AC test stimulus into the BSCs of the at least one driving IC;

scanning an initiate AC test instruction into the instruction register of both ICs;

performing an execute AC test instruction by moving the TAP controller to the *Run-Test/Idle* state and holding the TAP controller of both ICs in the *Run-Test/Idle* state for the time required to complete execution of the AC test instruction, wherein, during the *Run-Test/Idle* controller state, the at least one driving IC is applying the AC test stimulus to the at least one AC interconnection and the at least one receiving IC is sampling the signal;

transferring the results into the BSCs of the at least one receiving IC; and

scanning out the captured results.

10. The computer-readable medium as defined in claim 9, wherein the method further comprises the step of evaluating the captured AC test instruction results.

11. The computer-readable medium as defined in claim 9, wherein the method further comprises the step of generating a second AC test stimulus and repeating the steps of shifting, scanning, performing, transferring and scanning out with the second AC test stimulus.

12. The computer-readable medium as defined in claim 11, wherein the method further comprises the step of evaluating the captured AC test instruction results for the second AC test stimulus.

13. A system of testing AC coupled interconnects comprising:

at least one driving IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller;

at least one receiving IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller; and

at least one AC interconnection that couples the at least one driving IC to the at least one receiving IC;

wherein the BSCs of the at least one driving IC are capable of receiving an AC test stimulus, the instruction register of both ICs are capable of receiving an initiate AC test instruction, the TAP controller of both ICs is capable of being moved to and held in the *Run-Test/Idle* state for the time required to complete execution of the AC test instruction, wherein, during the *Run-Test/Idle* controller state, the at least one driving IC is applying the AC test stimulus to the at least one AC interconnection and the at least one receiving IC is sampling the signal, and the BSCs of the at least one receiving IC are capable of receiving and scanning out the captured results.

14. An *AC_Test_Marker* signal generator comprising:

a first shift register having a data input connected to a first signal line and a clock input connected to a second signal line;

a second shift register having a clock input connected to the second signal line;

a third shift register having an inverted clock input connected to the second signal line;

an AND gate having a first input connected to the first signal line, a second input connected to an inverted output of the first shift register, and an output connected to a data input of the second shift register; and

an OR gate having a first input connected to both an output of the second shift register and a data input of the third shift register, a second input connected to an output of the third shift register, and an output for the signal generator.

15. An *AC_Pattern_Source* signal generator comprising a shift register having a data input connected to an inverted output, a shift input connected to a first signal line, a clock input connected to a second signal line, and an output for the generator.

16. An *AC_Test_Ran* signal generator comprising a shift register having a shift input connected to a first signal line, a data input connected to a second signal line, a clock input connected to an *UpdateDR* signal line, a reset input connected to a *Reset* signal line, and an output for the generator.

17. An AC boundary scan cell comprising:

a first multiplexer having a system input connected to an SDI line, an output connected to an SDO line, and a select input connected to a first signal input line;

a second multiplexer having a system input also connected to the SDI line, an update input connected to a TDI line, and a select input connected to a *ShiftDR* signal input line;

a first data shift register having a data input connected to an output of the second multiplexer and a clock input connected to a second signal input line;

a second data register having a data input connected to both an output of the first data shift register and a TDO line and a clock input connected to an *UpdateDR* signal input line;

an XOR logic gate having a first input connected to an inverted output of the second data register and a second input connected to a third signal input line; and

a third multiplexer having a system input connected to an output of the second data register, an update input connected to an output of the XOR logic gate, a select input connected to a fourth signal input line, and an output connected to an update input of the first multiplexer.

18. An AC boundary scan cell comprising:

a first multiplexer having a system input connected to an SDI line, an output connected to an SDO line, and a select input connected to a first signal input line;

a second multiplexer having a system input also connected to the SDI line, an update input connected to a TDI line, and a select input connected to a *ShiftDR* signal input line;

a third multiplexer having a system input connected to an output of the second multiplexer and a select input connected to a second signal input line;

a first data shift register having a data input connected to an output of the third multiplexer and a clock input connected to a third signal input line;

a fourth multiplexer having a system input connected to an inverted output of the first data shift register, a select input connected to a fourth signal input line, and an output connected to an update input of the third multiplexer;

a second data register having a clock input connected to an *UpdateDR* signal input line; and

a fifth multiplexer having a system input connected to both an output of the second data register and an update input of the fourth multiplexer, an update input connected to each of an output of the first data shift register, a data input of the second

data register, and a TDO line, a select input connected to the second signal input line, and an output connected to an update input of the first multiplexer.

19. An AC boundary scan cell comprising:

a first multiplexer having a system input connected to an SDI line, an output connected to an SDO line, and a select input connected to a first signal input line;

a second multiplexer having a system input also connected to the SDI line, an update input connected to a TDI line, and a select input connected to a *ShiftDR* signal input line;

a third multiplexer having a system input connected to an output of the second multiplexer and a select input connected to a second signal input line;

a first data shift register having a data input connected to an output of the third multiplexer, a clock input connected to a third signal input line, an inverted output connected to an update input of the third multiplexer, and a shift input connected to a fourth signal input line;

a second data register having a clock input connected to an *UpdateDR* signal input line;

an XOR logic gate having a first input connected to an inverted output of the second data register and a second input connected to each of an output of the first data shift register, a data input of the second data register, and a TDO line; and

a fourth multiplexer having a system input connected to an output of the second data register, an update input connected to an output of the XOR logic gate, a select input

connected to the second signal input line, and an output connected to an update input of the first multiplexer.

20. An input AC boundary scan cell comprising:

a first multiplexer having a system input connected to an SDRI line, a select input connected to a first signal input line, and an output connected to an SDRO line;

a first data shift register having a data input connected to the SDRI line and a clock input connected to a second signal input line;

a second multiplexer having a system input connected to the SDRI line, an update input connected to an output of the first data shift register, and a select input connected to a third signal input line;

a third multiplexer having a system input connected to an output of the second multiplexer, an update input connected to a TDI line, and a select input connected to a *ShiftDR* signal input line;

a second data register having a dada input connected to an output of the third multiplexer and a clock input connected to a *ClockDR* signal input line; and

a third data shift register having a data input connected to both an output of the second data register and a TDO line, a clock input connected to an *UpdateDR* signal input line, and an output connected to an update input of the first multiplexer.

21. An input AC boundary scan cell comprising:

a first data shift register having a data input connected to an SDRI line and a clock input connected to a first signal input line;

a first multiplexer having a system input connected to an SDRO line, an update input connected to an output of the first data shift register, and a select input connected to a second signal input line;

a second multiplexer having a system input connected to an output of the first multiplexer, an update input connected to a TDI line, and a select input connected to a *ShiftDR* signal input line; and

and a second data register having a data input connected to an output of the second multiplexer, a clock input connected to a *ClockDR* signal input line, and an output connected to a TDO line.

22. A bi-directional AC boundary scan cell comprising:

an output cell comprising:

a first multiplexer having a system input connected to an SDI line, an output connected to an SDO line, and a select input connected to a *Mode* signal input line;

a second multiplexer having a system input also connected to the SDI line and a select input connected to a *ShiftDR* signal input line;

a first data shift register having a data input connected to an output of the second multiplexer and a clock input connected to a first signal input line;

a second data register having a data input connected to both an output of the first data shift register and a TDO line and a clock input connected to an *UpdateDR* signal input line;

an XOR logic gate having a first input connected to an inverted output of the second data register and a second input connected to a second signal input line; and

a third multiplexer having a system input connected to an output of the second data register, an update input connected to an output of the XOR logic gate, a select input connected to a third signal input line, and an output connected to an update input of the first multiplexer; and

an input cell comprising:

a third data shift register having a data input connected to an SDRO line and a clock input connected to a fourth signal input line;

a fourth multiplexer having a system input connected to an SDRI line, an update input connected to an output of the third data shift register, and a select input connected to a fifth signal input line;

a fifth multiplexer having a system input connected to an output of the fourth multiplexer, an update input connected to a TDI line, and a select input connected to a *ShiftDR* signal input line; and

and a fourth data register having a data input connected to an output of the fifth multiplexer, a clock input connected to a *ClockDR* signal input line, and an output connected to an update input of the second multiplexer of the output cell.

23. A bi-directional AC boundary scan cell comprising:

a first multiplexer having a system input connected to an SDI line, a select input connected to a *Mode* signal input line, and an output connected to an SDO line;

a first data shift register having a data input connected to an SDRO line and a clock input connected to a first signal input line;

a second multiplexer having a system input connected to an output of the first data shift register, an update input also connected to an SDRI line, and a select input connected to a second signal input line;

a third multiplexer having a system input connected to an output of the second multiplexer, and update input connected to a TDI line, and a select input connected to a *ShiftDR* signal input line;

a second data register having a data input connected to an output of the third multiplexer and a clock input connected to a *ClockDR* signal input line;

a third data shift register having a data input connected to both an output of the second data register and a TDO line and a clock input connected to an *UpdateDR* signal input line;

an XOR logic gate having a first input connected to an inverted output of the third data shift register and a second input connected to a third signal input line;

and a fourth multiplexer having a data input connected to an output of the third data shift register, an update input connected to an output of the XOR logic gate, a select input connected to a fourth signal input line, and an output connected to an update input of the first multiplexer.

24. A bi-directional AC boundary scan cell comprising:

a first multiplexer having a system input connected to an SDI line, a select input connected to a *Mode_1* signal input line, and an output connected to an SDO line;

a second multiplexer having a system input connected to an SDRO line, an update input connected to an update input of the first multiplexer, and a select input connected to a *Mode_2* signal input line;

a first data shift register having a data input connected to an output of the second multiplexer and a clock input connected to a first signal input line;

an AND logic gate having an inverted input also connected to the *Mode_1* signal input line;

a third multiplexer having a system input also connected to the output of the second multiplexer, and update input connected to an output of the first data shift register, and a select input connected to a second signal input line;

a fourth multiplexer having a system input connected to an output of the third multiplexer, an update input connected to an output of the first multiplexer, and a select input connected to an output of the AND logic gate;

a fifth multiplexer having a system input connected to an output of the fourth multiplexer, an update input connected to a TDI line, and a select input connected to a *ShiftDR* signal input line;

a second data register having a data input connected to an output of the fifth multiplexer and a clock input connected to a *ClockDR* signal input line;

a third data register having a data input connected to both an output of the second data register and a TDO line and a clock input connected to an *UpdateDR* signal input line;

a XOR logic gate having a first input connected to an inverted output of the third data register and a second input connected to a third signal input line; and

a sixth multiplexer having a system input connected to an output of the third data register, an update input connected to an output of the XOR logic gate, a select input connected to a fourth signal input line, and an output also connected to the update input of the first multiplexer.

25. A system of testing AC coupled interconnects having at least one AC interconnection and at least one driving IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller, wherein the BSCs of the at least one driving IC are capable of receiving an AC test stimulus, the instruction register of the at least one driving IC is capable of receiving an initiate AC test instruction, and the TAP controller of the at least one driving IC is capable of being moved to and held in the *Run-Test/Idle* state for the time required to complete execution of the AC test instruction, the system comprising:

at least one receiving IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller, wherein the at least one AC interconnection couples the at least one driving IC to the at least one receiving IC, the instruction register of the at least one receiving IC is capable of receiving an initiate AC test instruction, the TAP controller of the at least one receiving IC is capable of being moved to and held in the *Run-Test/Idle* state for the time required to complete execution of the AC test instruction, wherein, during the *Run-Test/Idle* controller state, the at least one driving IC is applying the AC test stimulus to the at least one AC interconnection and the at least one receiving IC is sampling the signal, and the BSCs of the at least one receiving IC are capable of receiving and scanning out the captured results.

26. A system of testing AC coupled interconnects having at least one AC interconnection and at least one receiving IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller, wherein the instruction register of the at least one receiving IC is capable of receiving an initiate AC test instruction, the TAP controller of the at least one receiving IC is capable of being moved to and held in the *Run-Test/Idle* state for the time required to complete execution of the AC test instruction, the at least one receiving IC is capable of sampling a signal, and the BSCs of the at least one receiving IC are capable of receiving and scanning out the captured results, the system comprising:

at least one driving IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller, wherein the at least one AC interconnection couples the at least one driving IC to the at least one receiving IC, the BSCs of the at least one driving IC are capable of receiving an AC test stimulus, the instruction register of the at least one driving IC is capable of receiving an initiate AC test instruction, the TAP controller of the at least one driving IC is capable of being moved to and held in the *Run-Test/Idle* state for the time required to complete execution of the AC test instruction, and wherein, during the *Run-Test/Idle* controller state, the at least one driving IC is applying the AC test stimulus to the at least one AC interconnection and the at least one receiving IC is sampling the signal.